

REMARKS

Claims 1-30 were pending prior to amendment. Claims 1-6 and 9-29 stand rejected as allegedly being anticipated by U.S. Patent No. 4,371,932 to Dinwiddie et al. ("Dinwiddie"). Claims 7 and 30 stand rejected as allegedly being unpatentable over Dinwiddie in view of U.S. Patent No. 5,784,699 to McMahon ("McMahon"). Claim 8 stands rejected under 35 U.S.C. 103(a) as allegedly being unpatentable over Dinwiddie in view of U.S. Patent No. 5,546,554 to Young et al. ("Young").

Claims 1-30 have been cancelled. New claims 34-50 have been added. New claims 34-50 are supported in the specification; see, for example, page 4, lines 3-21. In view of the remarks below, Applicant respectfully traverses the rejections and asks that they be withdrawn. Reconsideration and allowance are respectfully requested.

I. The Rejections under 35 U.S.C. 102(b) and 103(a)

Applicant has cancelled claims 1-30 and added new claims 34-50 to more clearly emphasize the patentable aspects of Applicant's disclosure. For example, claims 34-50 recite a storage capacity for the multi-ported memory, in order to obviate any interpretation which would read the multi-ported memory as elements, such as registers, providing minimal storage. Additionally, claims 34-50 more clearly emphasize that

a memory location is determined based (at least in part) on whether a control/status access or a data access is desired.

Systems and techniques described in the current disclosure allow for more efficient memory use in a number of ways. For example, routing control/status accesses to the multi-ported memory rather than the main memory avoids bus snooping, and thus reduces the related performance degradation (please see, e.g., page 3 line 22 to page 4 line 2 of the specification).

Additionally, since the main memory may handle data accesses more efficiently than control/status accesses (e.g., when the main memory is implemented using RDRAM, please see page 3, lines 14-15 of the specification), routing control/status accesses to the multi-ported memory allows more efficient use of the main memory.

In contrast, Dinwiddie does not teach determining a memory destination between the main memory or the multi-ported memory based on the information type (e.g., based on whether the information is control/status information or data). Instead, Dinwiddie teaches an input/output (I/O) controller for transferring data between a host processor and one or more I/O devices (please see the Abstract of Dinwiddie). According to Dinwiddie, "All data transfers are by way of the dual port storage unit," (please see the Abstract of Dinwiddie, emphasis

added) where the data transfers referred to are data transfers between a host processor and one or more I/O devices.

As noted in previous responses, it appears that any modification of Dinwiddie to include the features of claims 34-50 would render Dinwiddie unsatisfactory for its intended purpose. When a proposed modification would render the prior art invention being modified unsatisfactory for the intended purpose, then there is no suggestion or motivation to make the proposed modification (see MPEP 2143.01). If Dinwiddie were modified so that only control/status accesses were directed to mechanism 22, it would no longer function as a data transfer interface between the microprocessor bus and the host processor channel bus for all data. Since Dinwiddie describes this data transfer interface as "A primary feature of the new and improved I/O controller 2," (see column 4, lines 59-60 of Dinwiddie), any interpretation that requires modifying Dinwiddie so that control accesses are no longer directed to mechanism 22 is improper, per MPEP 2143.01.

For at least the above reasons, claims 34-50 are patentable over Dinwiddie.

#### CONCLUSION

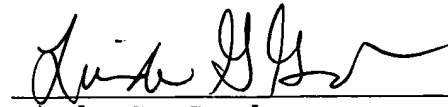
In view of the above remarks, claims 34-50 are in condition for allowance.

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Respectfully submitted,

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